

Analog IP Reuse

A methodology to map analog IP's to different foundries

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About IQ-Analog



The screenshot shows a search interface for IP blocks. At the top, there are three tabs: "Search for IP" (selected), "View All", and "Custom IP Request". Below the tabs, there are several search criteria:

- Keywords:** A text input field.
- Function:** Three buttons labeled "ADC", "DAC", and "AFE".
- Resolutions (bits):** A range of "10 - 16 Bits" with a horizontal slider bar below it.
- Speed (MHz):** A range of "10 - 800 MHz" with a horizontal slider bar below it.
- Foundry:** A grid of buttons for various foundries: TSMC, SMIC, UMC, IBM, Global Foundries, TowerJazz, Toshiba, Fujitsu, and Silterra.
- Node (nm):** A row of buttons for different technology nodes: 180, 130, 90, 65, 40, and 28.

At the bottom of the form is a large orange "SUBMIT" button.

IQ-Analog offers a full portfolio of “off-the-shelf” data converter intellectual property (IP) in multiple foundries with proven silicon performance. We also provide custom AFE technology that is tailored to customer needs.

Our Challenge

- ❑ Customers have different requirements, use different foundries/ processes - **technology is always moving**
- ❑ Most delivered IP requires customization
 - Unique customer functional requirements
 - Back end of line (BEOL) metal stack variations
 - New foundry and/or technology node
- ❑ Tight delivery schedules are required
 - Existing designs must be fully leveraged
- ❑ Analog IP porting challenges
 - Availability of the same (or similar) active and passive components
 - Different DRC rules drive manual physical layout modifications
 - Different BEOL drive manual physical layout modifications
 - **Design update + verification iterative cycle delays**

Our Recipe

- ❑ Couple EDA tools to data management tools to keep track of various versions of IP content including schematics, layout, simulation setups, technology kits, etc.
- ❑ Leverage the use of an organized library with numerous tags & branches to assemble the targeted IP core
- ❑ Per customer requirements, establish the project configuration to efficiently leverage our ever-growing library of IP content without redundancies.

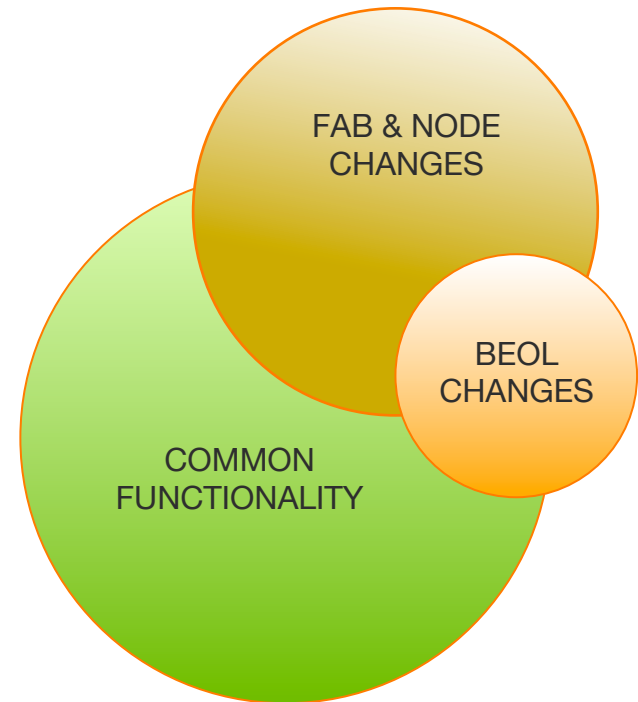
- ❑ **IQ-Analog uses ClioSoft's SOS data management platform:**
 - Workspace follows a strict rule based system using tags and branches
 - Tags are used to represent meaningful development milestones
 - Branches are used to represent alternative development paths

Variant Management Challenges

- ❑ Changes happen on multiple axes
 - Common functionality updates
 - Fab and node changes
 - Back-end-of-line changes

- ❑ Need to pick changes from multiple lines of development
 - Changes are dynamic with multiple active designers operating on the same data

- ❑ Need to reliably select a **coherent** set of changes



SOS Features Used

❑ Tagging

- Labeling a revision with a meaningful name
- A revision of a file may have multiple tags
- A tag on a file can be moved to a different revision

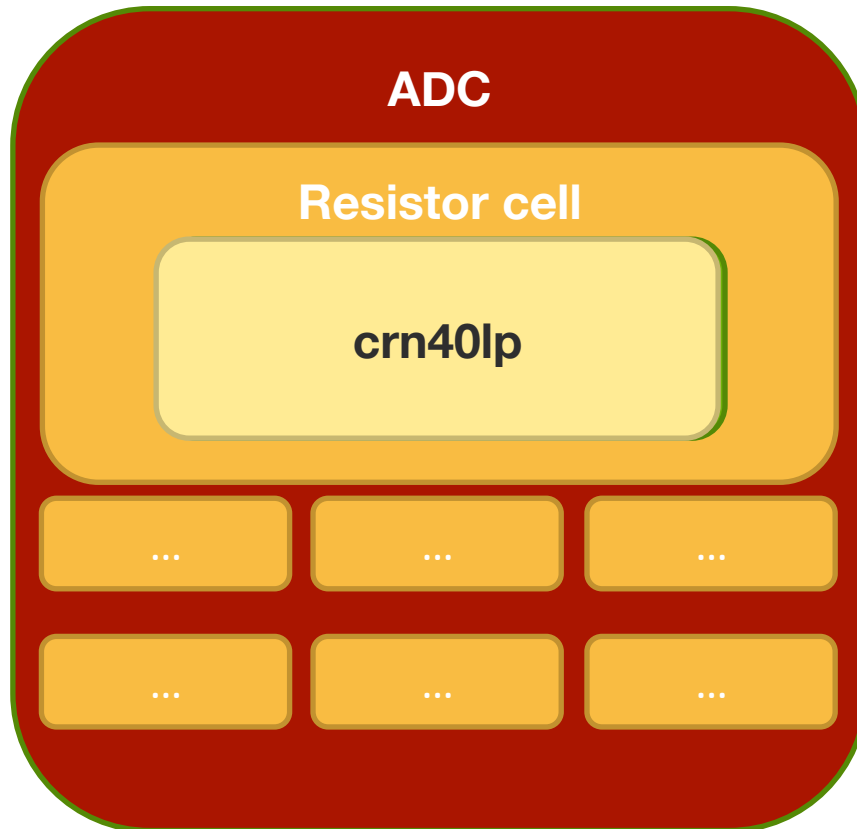
❑ Branching

- Ability to create an alternative path of development
- Sub-branches can be created off branches
- All branches of development are visible to all, allowing changes on multiple branches to be selected

❑ Revision search order (RSO)

- A priority ordered list of tag and branch names
- A rule to pick revisions to create a workspace
- Revision with the first matching tag or branch name is selected

ADC sub-component Example



- ❑ An ADC cell has a poly resistor component
- ❑ The initial Implementation is with a specific fab, say “gf40”
- ❑ Technology libraries are created for all anticipated fabs segregated by branches and/or tags.
- ❑ We want to move to a new fab so we just update the RSO with the new reference libraries
- ❑ The updated resistor now references the proper cell for the “crn40lp” fab

Simple Example: Poly resistor

RSO (original)

iqa40_crn40_7m4x2z
iqa40_crn40
iqa40

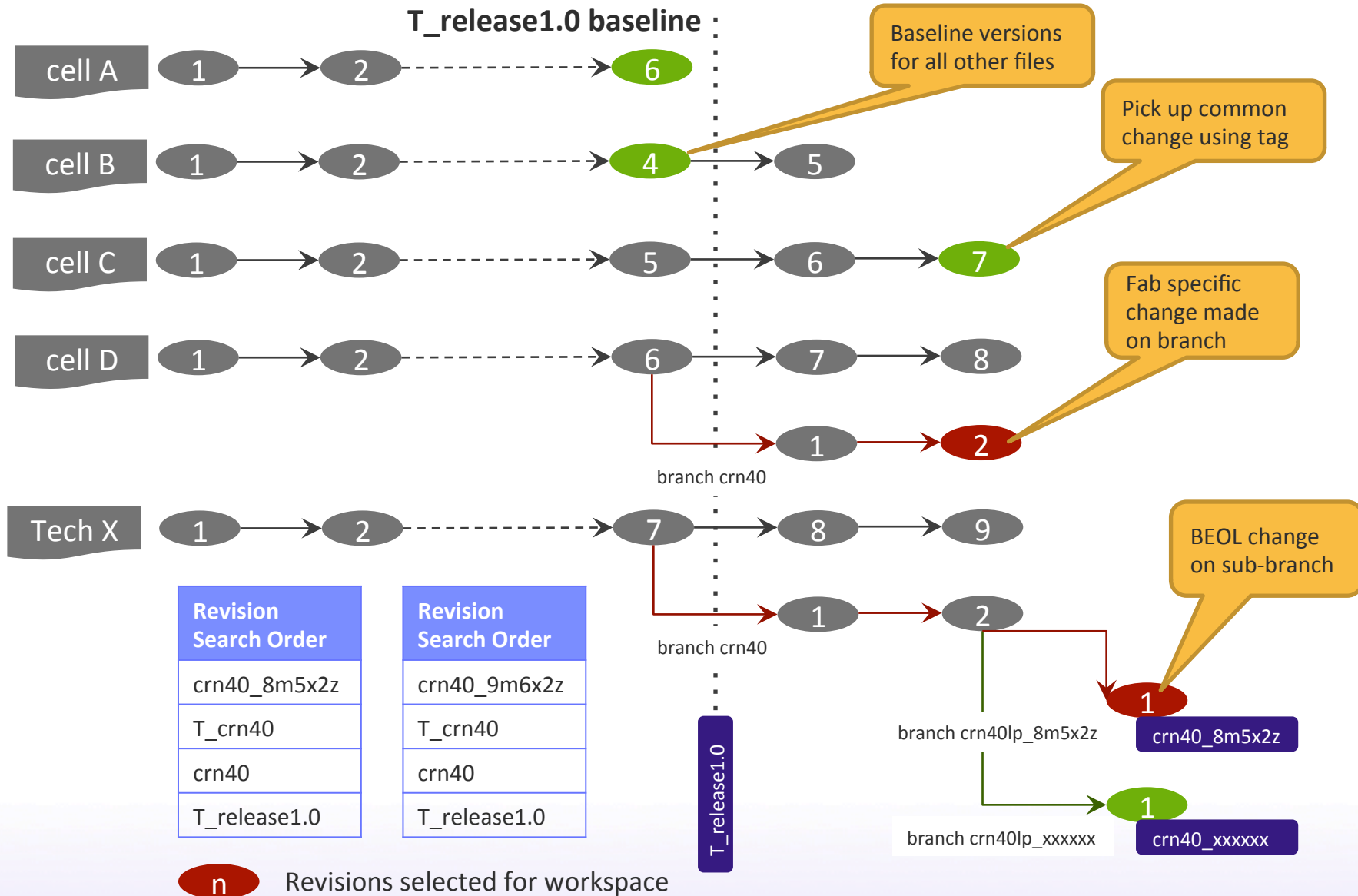
RSO

iqa40_cmos11lp_6L1x2T6xLB
iqa40_cmos11lp
iqa40



New internal dimensions for contact to blockage
New marking layers
SAME physical connection points
SAME electrical properties

Configuration Example

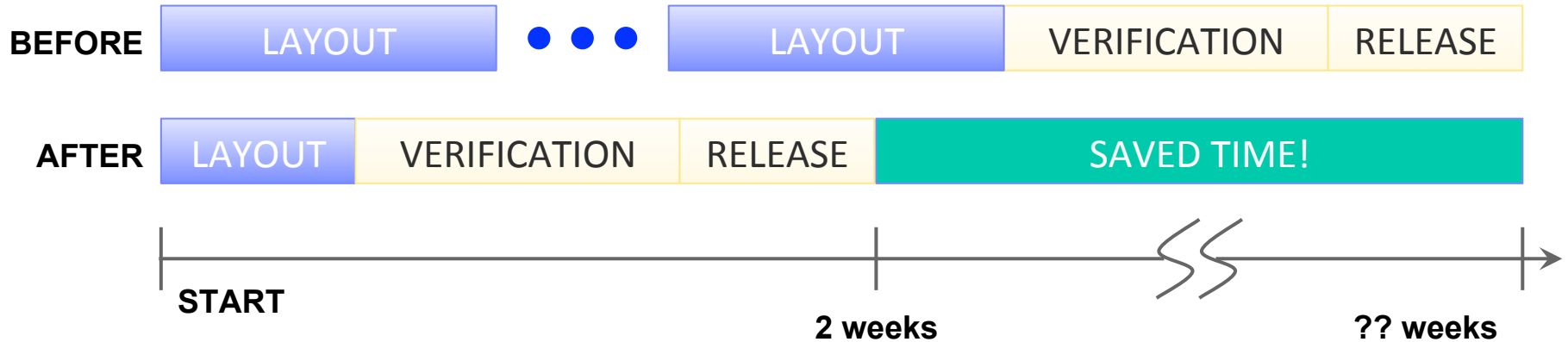


Revision Search Order
crn40_8m5x2z
T_crn40
crn40
T_release1.0

Revision Search Order
crn40_9m6x2z
T_crn40
crn40
T_release1.0

Evidence

- ❑ How long does it take to migrate from one tech to another?



- ❑ Retargeting IP from TSMC 40nm to GlobalFoundries 40nm took just 2 weeks.
 - IP contained resistors, capacitors and related analog components. These were already prepared in technology library allowing for a rapid transition and then verification of the results
- ❑ Retargeting from TSMC's 40nm BEOL of 5x2x to 6x2z took just 2 days
 - Able to maintain TSMC branch and only branched further the layout views in which the metal transitioned above the thin metals

Summary

- ❑ Using ClioSoft's SOS data management tool with a strict methodology of tagging and branching allows us to be more productive and efficient
 - The greatest advantage is realized when a designer might need to augment only a few items to implement a fix rather than traversing all implementations to incorporate fixes and corrects.
 - Changing the underlying reference and then re-running verification may be all that is needed for a delivery

- ❑ Automating the process to reduce the time required to map an analog IP from one foundry node to another is of great value (to us)
 - The upfront work of creating the content in a given node facilitates a designer to implement fixes in all the nodes instantly saving the time it would take to implement the changes uniquely in each project
 - This automation avoids "clerical" errors which can be introduced in manual efforts to mapping from one node to another

Thank You!

